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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/527,220	09/27/2005	Hiromichi Hayase	2005_0403A	3231
513 7590 06/28/2007 WENDEROTH, LIND & PONACK, L.L.P. 2033 K STREET N. W. SUITE 800 WASHINGTON, DC 20006-1021			EXAMINER NGUYEN, PATRICIA T	
			ART UNIT 2817	PAPER NUMBER
			MAIL DATE 06/28/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/527,220	Applicant(s) HAYASE, HIROMICHI	
	Examiner Patricia T. Nguyen	Art Unit 2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-17 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-4, 6, 7, 11-14, 16 and 17 is/are rejected.
- 7) ☒ Claim(s) 5, 8-10 and 15 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>3/9/05</u> . | 6) <input type="checkbox"/> Other: ____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4, 7, 11-14, and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Mucenieks, U.S. Patent # 6,359,508 B1.

Fig. 1 of Mucenieks discloses a circuit comprising: distortion component amplitude detection means (88, 97) that detects an amplitude of a distortion component produced by an amplifier (10) contained in a signal (RFin) amplified by an amplifier (10) after distortion compensation (25), and amplified signal level reduction control means (DSP 30) that in a case in which the amplitude of the distortion component detected by the distortion component amplitude detection exceeds a predetermined threshold value, performs control to reduce the level of the signal amplified by the amplifier(10). Pre-d 25 can be read as predistortion means; DSP 30 can be read as predistortion control means; variable attenuator 21 can be read as a variable attenuator provided in the stage before the amplifier; variable attenuator 61 can be read as a variable attenuator provided in the stage after the amplifier.

Claims 1-3, 7, 11-13, and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Funada et al., U.S. Patent # 6,417,731 B1.

Fig. 1 of Funada et al. discloses a circuit comprising: distortion component amplitude detection means (12) that detects an amplitude of a distortion component produced by an amplifier (4) contained in a signal (input) amplified by an amplifier (4) after distortion compensation (3), and amplified signal level reduction control means (13) that in a case in which the amplitude of the distortion component detected by the distortion component amplitude detection exceeds a predetermined threshold value, performs control to reduce the level of the signal amplified by the amplifier. Predistorter 3 can be read as predistortion means; control circuit 13 can be read as predistortion control means; vector adjuster 2 can be read as a variable attenuator.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 6, 11-13, and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Horaguchi et al., U.S. Patent # 6,925,106 B2.

Fig. 1 of Horaguchi et al. discloses a circuit comprising: distortion component amplitude detection means (5) that detects an amplitude of a distortion component produced by an amplifier (2) (see spec. col. 11, lines 42-50) contained in a signal (input) amplified by an amplifier (2) after distortion compensation (1), and amplified signal level reduction control means (10) that in a case in which the amplitude of the distortion component detected by the distortion component amplitude detection exceeds a predetermined threshold value, performs control to reduce the level of the signal

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amplified by the amplifier. Predistortion unit 1 can be read as predistortion means; control circuit 10 can be read as predistortion control means; attenuator 11 can be read as a variable attenuator.

Allowable Subject Matter

Claims 5, 8-10, 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Patricia T. Nguyen whose telephone number is (571) 272-1768. The examiner can normally be reached on 6:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on 571-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PTN

June 25, 2007



PATRICIA NGUYEN
PRIMARY EXAMINER